AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

1. (currently amended) A method of plating an electrical contact on a ~~printed wiring board~~ substrate, comprising:

forming a metal interconnect ~~trace~~ on first and second opposing sides of a ~~printed wiring board~~ substrate and through a via formed through the ~~printed wiring board~~ substrate;

forming first and second dielectric layers on the metal interconnect ~~trace~~ and over the first and second sides of the ~~printed wiring board~~ substrate, respectively, wherein the first and second dielectric layers each have openings therethrough that expose portions of the metal interconnect ~~trace~~;

forming first and second plating layers on the first and second dielectric layers, respectively, and ~~one~~ on the sides of the openings and on the exposed portions of the metal interconnect ~~trace~~, the first and second plating layers electrically connected by the metal interconnect ~~trace~~;

electroplating first and second contact layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second dielectric layers while leaving the portions of the first and second plating layers under the first and second contact layers.

2. (currently amended) The method as recited in Claim 1 wherein forming first and second plating layers includes forming the first and second plating layers with an electro-less process and the method further includes electroplating first and second conductive layers on the first and second plating layers, respectively.

3. (currently amended) The method as recited in Claim 1 wherein electroplating first and second contact layers includes electroplating first and second barrier layers over the first and second plating layers, respectively.

D1 Cont'd

4. (currently amended) The method as recited in Claim 3 wherein electroplating first and second barrier layers includes electroplating first and second nickel layers, respectively, and electroplating first and second contact layers further includes electroplating first and second gold layers on the first and second nickel layers, respectively.

5. (currently amended) The method as recited in Claim 1 wherein forming the first plating layer includes forming a discontinuous first plating layer.

6. (currently amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer prior to electroplating the first and second contact layers.

7. (currently amended) The method as recited in Claim 1 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer subsequent to electroplating the first and second contact layers.

8. (currently amended) A method of manufacturing an integrated circuit (IC) substrate, comprising:

forming a multi-layered substrate with a printed wiring board core and having vias formed therethrough;

forming metal interconnects ~~traces~~ on first and second opposing sides of the printed wiring board and through the vias;

forming first and second dielectric layers on the metal interconnects ~~traces~~ over the first and second sides of the printed wiring board, respectively, the first and second dielectric layers each having openings therethrough that expose portions of the metal interconnects ~~traces~~; and

plating an electrical contact on the substrate, including:

forming first and second plating layers on the first and second dielectric layers, respectively, and on the sides of the openings and on the exposed portions of the metal interconnects ~~traces~~, the first and second plating layers electrically connected by one of the metal interconnects ~~traces~~;

electroplating first and second contact layers over a respective portion of each of the first and second plating layers using the first and second plating layers; and

removing a portion of each of the first and second plating layers from the first and second dielectric layers while leaving the portions of the first and second plating layers under the first and second contact layers.

9. (currently amended) The method as recited in Claim 8 wherein forming the first and second plating layers includes forming the first and second plating layers with an electro-less process and the method further includes electroplating first and second conductive layers on the first and second plating layers, respectively.

D1 Cont'd

10. (currently amended) The method as recited in Claim 8 wherein electroplating first and second contact layers includes electroplating first and second barrier layers over the first and second plating layers, respectively.

11. (currently amended) The method as recited in Claim 10 wherein electroplating first and second barrier layers includes electroplating first and second nickel layers and electroplating first and second contact layers further includes electroplating first and second gold layers on the first and second nickel layers.

12. (currently amended) The method as recited in Claim 8 wherein forming the first plating layer includes forming a discontinuous first plating layer.

13. (currently amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the first plating layer prior to electroplating the first and second contact layers.

14. (currently amended) The method as recited in Claim 8 wherein removing a portion of each of the first and second plating layers includes removing a portion of the second plating layer subsequent to electroplating the first and second contact layers.

D 1, Cont'd

Claims 15-20 (canceled).

21. (previously presented) The method as recited in Claim 1 wherein the first and second plating layers are not formed in the via.

22. (currently amended) The method as recited in Claim 2 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the openings.

23. (previously presented) The method as recited in Claim 8 wherein the first and second plating layers are not formed in the vias.

D1 Cont'd

24. (previously presented) The method as recited in Claim 9 wherein the electroplating first and second conductive layers includes electroplating first and second conductive layers each substantially confined to the openings.